16.9 Laser Radar Imager Based on 3D Integration of Geiger-Mode Avalanche Photodiodes with Two SOI Timing Circuit Layers

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We have developed focal-plane arrays and laser-radar (ladar) imaging systems based on Geiger-mode avalanche photodiodes (APDs) integrated with high-speed all-digital CMOS timing circuits. A Geiger-mode APD produces a digital pulse upon detection of a single photon. This pulse is used to stop a fast digital counter in the pixel circuit, thereby measuring photon arrival time. This "photon-to-digital conversion" yields quantum-limited sensitivity and noiseless readout, enabling high-performance ladar systems. Previously reported focal planes, based on bump bonding or epoxy bonding the APDs to foundry chips, had coarse (100μm) pixel spacing and 0.5ns timing quantization. [1]

We have developed a fully depleted SOI CMOS fabrication process and techniques to fabricate three-dimensional integrated circuits by stacking SOI wafers to form multiple "tiers" of circuitry interconnected with micron-scale vias [2]. Such a 3D integration process could enable new computing architectures that exploit short, massively parallel interconnections between tiers.

CMOS imagers are another beneficiary of this process; multiple tiers of circuitry behind the photodetector facilitate on-focal-plane processing with a small pixel footprint. We present here a 3D-integrated 3-tier 64×64 ladar focal plane with 50μm pixel spacing and circuitry *added* to the pixel to refine the timing quantization.

Figure 16.9.1 is a block diagram of the chip and Fig. 16.9.2 shows the pixel circuit detail. Figure 16.9.1 also shows the partitioning of functions among the three tiers. Tier 1 is a bulk wafer with an epitaxial layer in which the Geiger-mode APD array is fabricated. Tier 2, fabricated in a 3.3V, 0.35μm SOI process, includes circuitry that charges the cathode of the APD to a logic-high state. When the APD detects a photon, it discharges, bringing its cathode to a logic-low state, thereby generating a stop signal for the timing circuitry. Tier 3, fabricated in a 1.5V, 0.18μm SOI process, includes a 9b pseudorandom counter [3]. A timing clock is generated by a 9-stage ring oscillator at the periphery of the focal plane on tier 3; one of the stages is a NAND gate, allowing the ring oscillator to be enabled by the start signal for the photon-flight-time measurement. This clock is broadcast through a buffer tree to all 64 rows of the focal plane. In each pixel, the clock passes through a tri-state inverter to operate the pseudorandom counter. The stop signal puts the tri-state inverter into the high-impedance state, stopping the counter and digitizing the photon arrival time to a resolution of one clock period. The clock is also fed into a chain of three inverters on tier 2, which functions as a delay line for fine timing resolution. The outputs of these inverters are captured by a 3b register in response to the stop signal. The state of this register encodes the clock phase at the time of photon detection. Readout of this register yields one of six valid patterns: 000, 100, 110, 111, 011, and 001, each of which maps to a delay-line state during the propagation of a rising or falling clock edge through the inverter chain. The ring oscillator is biased separately, allowing the clock frequency to be adjusted so that the edge propagation delay through the delay line corresponds to half the clock period. Based on SPICE simulations, this "matched" clock period is 600ps, corresponding to 100ps time quantization.

The pseudorandom counter is a 9b shift register with feedback paths that compute the input (Q0) as the XOR of bits Q4 and Q9. This architecture was chosen for its compact footprint. Use of combinatorial logic for the XOR and the MUX introduces a long delay in the feedback path that limits the counter's operational speed. Therefore, this feedback computation is pipelined. The XOR operation is done by the master stage of an additional flip-flop in the feedback path. The XOR circuit requires two inputs and their logical complements. The necessary inversions are pipelined using two additional flip-flops. The pipelined counter requires feedback taps at bits Q2, Q3, Q7 and Q8. Once the photon flight time is measured, a 2-to-1 MUX switches the data path so that the input to the shift register comes from the output of the neighboring pixel, and the rows are read out serially using an external clock (not shown in the figures). The MUX operation is carried out by the master stage of the Q1 flip-flop and uses the same circuit as the XOR.

The tier-2 circuitry includes a subcircuit to arm and disarm the APD and to generate the stop signal. The stop signal generates a clock edge that parallel loads the delay-line state into the register. During readout, the data and clocking paths are switched so that the tier-3 and tier-2 circuits form a single 12b shift register, and the pixels in each row are daisy chained for serial readout. The chip has 16 output ports, each with a 4-to-1 MUX to address four adjacent rows.

Figure 16.9.3 shows the 3D-integration process [2]. Each tier is added to the stack by low-temperature oxide-to-oxide bonding, and then the SOI handle wafer is removed. 1.5-μm-diameter connection vias to the underlying tier are made by anisotropic etching and standard via plug-fill techniques. An imager illuminated from the tier-1 side is made by thinning the APD substrate, patterning anode-contact metallization and etching streets around the periphery to expose the bonding pads. Figure 16.9.4 is a 3D CAD drawing of the pixel layout. Each pixel has 227 transistors and 6 3D vias. Figure 16.9.7 is a die micrograph of a focal-plane array.

The chip design includes a single 3D-integrated ladar pixel to test circuit components. This pixel is clocked by a dedicated ring oscillator located on tier 3. The pseudorandom counter operation was validated at 1.6GHz by varying the delay between the start signal to the ring oscillator and an externally-supplied stop signal, and ascertaining the correctness of the timing values read out. Another test component is the clock-phase capture circuit from tier 2. Figure 16.9.5 shows a plot of the probability of occurrence of each output pattern versus the delay between a falling clock edge and a stop signal, both externally supplied. Timing quantizations of 130ps and 110ps are obtained, respectively, for the rising and falling clock edges. Figure 16.9.6 shows a grayscale timing image and histogram from a 64×64 imager illuminated with a sub-ns pulse from a 684nm laser diode. Power distribution issues and a readout clock race condition constrained operation to a timing resolution of 2ns. This focal plane represents the first functional 3-tier circuit with active circuits and devices on all tiers.

References:

[1] B. Aull, "3D Imaging with Geiger-mode Avalanche Photodiodes," *Optics & Photonics News*, vol. 16, pp. 42-46, May, 2005.

[2] V. Suntharalingam et al., "Megapixel CMOS Image Sensor Fabricated in Three-Dimensional Integrated Circuit Technology," *ISSCC Dig. Tech. Papers*, pp. 16-17, Feb., 2005.

[3] S. Cowan, "Handbook of Digital Logic," Prentice-Hall Inc., 1985.

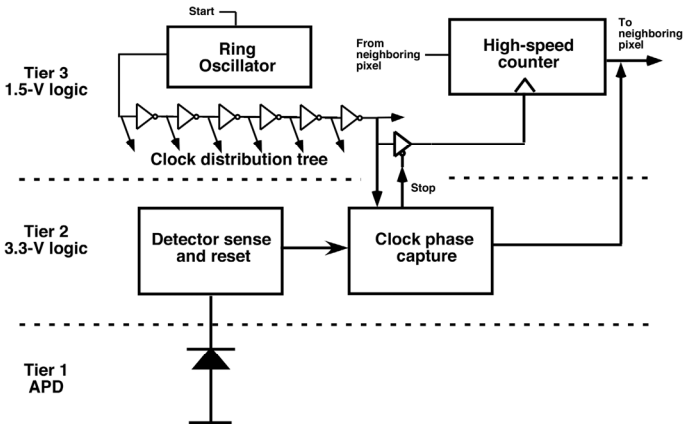

Figure 16.9.1: Chip block diagram.

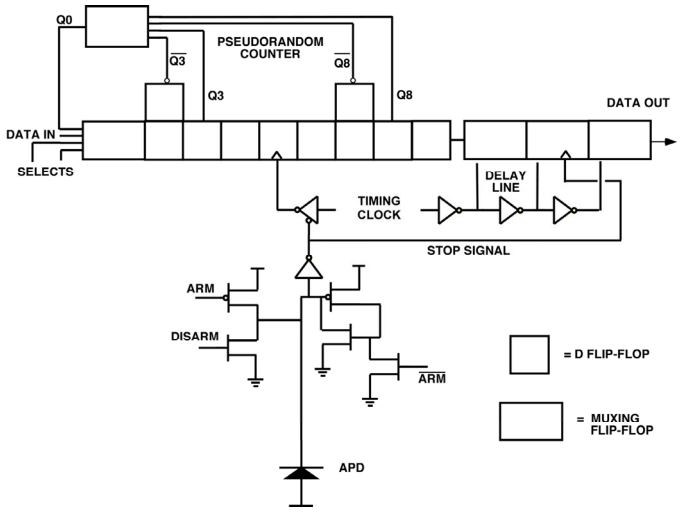

Figure 16.9.2: Pixel circuit detail.

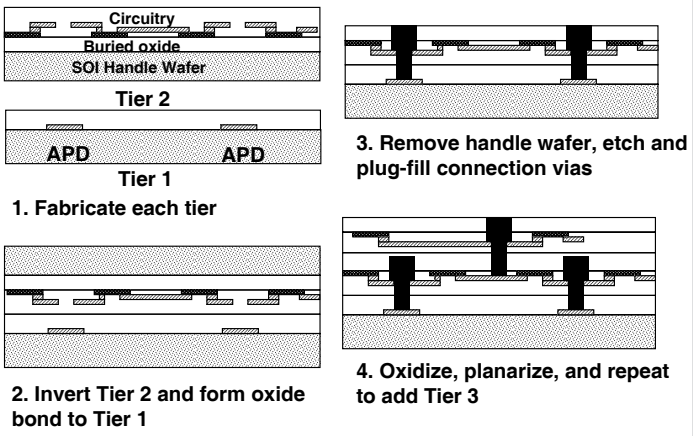

Figure 16.9.3: 3D integration process steps.

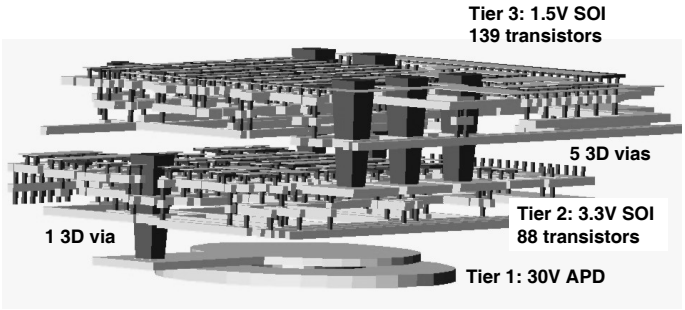

Figure 16.9.4: 3D CAD rendering of pixel layout.

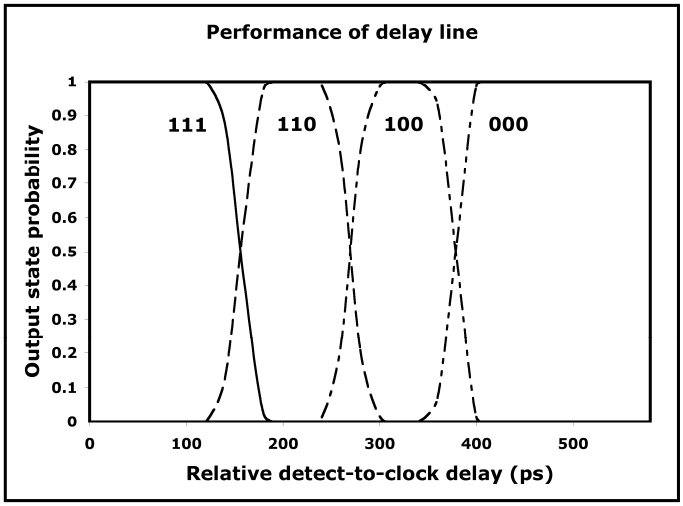

Figure 16.9.5: Delay-line performance.

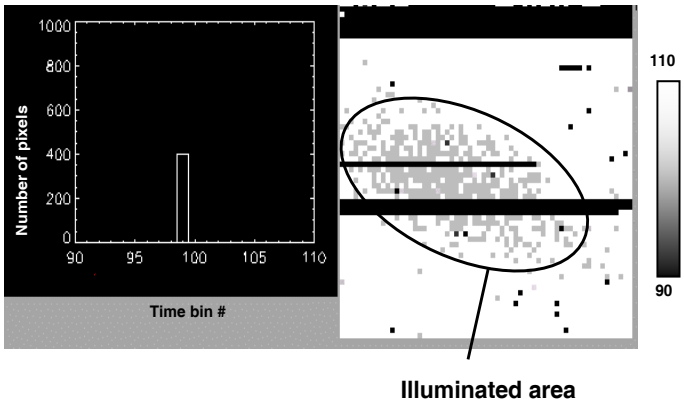

Figure 16.9.6: Timing image and histogram.

Continued on Page 655

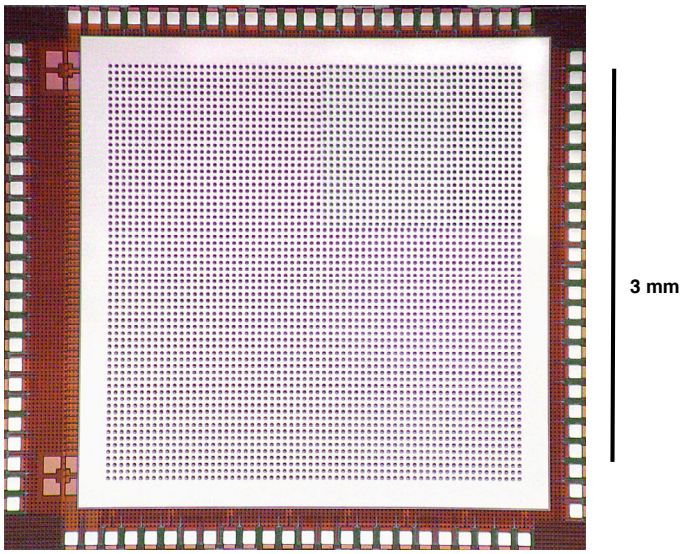

Figure 16.9.7: Imager die micrograph.

